National Semiconductor

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DS25BR440
3.125 Gbps Quad LVDS Buffer with Transmit Pre-Emphasis and Receive Equalization

General Description

The DS25BR440 is a 3.125 Gbps Quad LVDS buffer optimized for high-speed signal routing and repeating over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR440 features two levels of transmit pre-emphasis (PE) and two levels of receive equalization (EQ). Both of these features compensate for interconnect losses and ultimately maximize noise margin. A loss-of-signal ($\overline{LOS}$) circuit monitors each input channel and a unique $\overline{LOS}$ pin is asserted when no signal is detected at that input

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

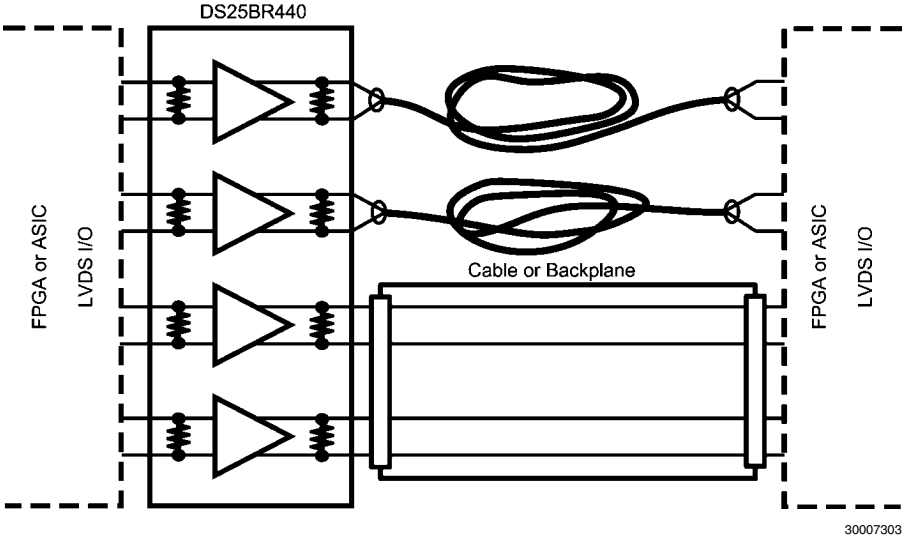
Features

- DC - 3.125 Gbps low jitter, low skew, low power operation
- Pin selectable transmit pre-emphasis and receive equalization eliminate data dependant jitter
- Wide input common mode voltage range allows DC-coupled interface to LVDS, CML and LVPECL drivers
- $\overline{LOS}$ circuitry detects open inputs fault
- Integrated 100Ω input and output terminations
- 8 kV ESD on LVDS I/O pins protects adjoining components
- Small 6 mm x 6 mm LLP-40 space saving package

Applications

- Clock and data buffering and repeating
- Copper cable driving and equalization
- FR-4 equalization
- OC-48 / STM-16

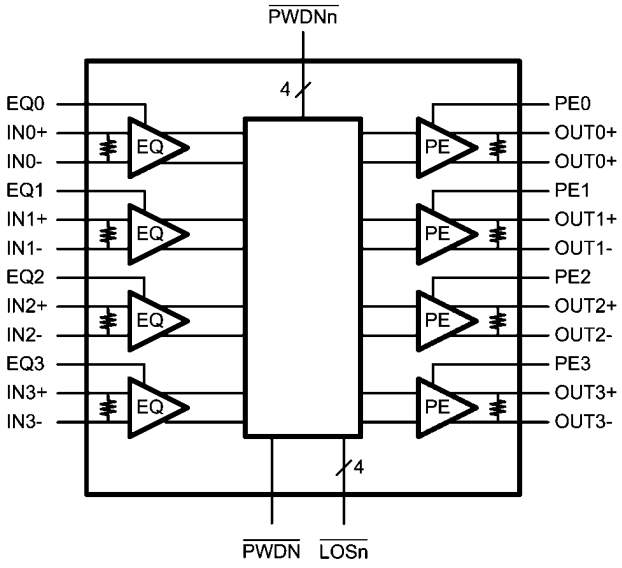
Typical Application



Ordering Code

NSID	Function	Available Equalization Levels	Available Pre-Emphasis Levels
DS25BR440TSQ	Quad Buffer / Repeater	Off / On	Off / On

Block Diagram



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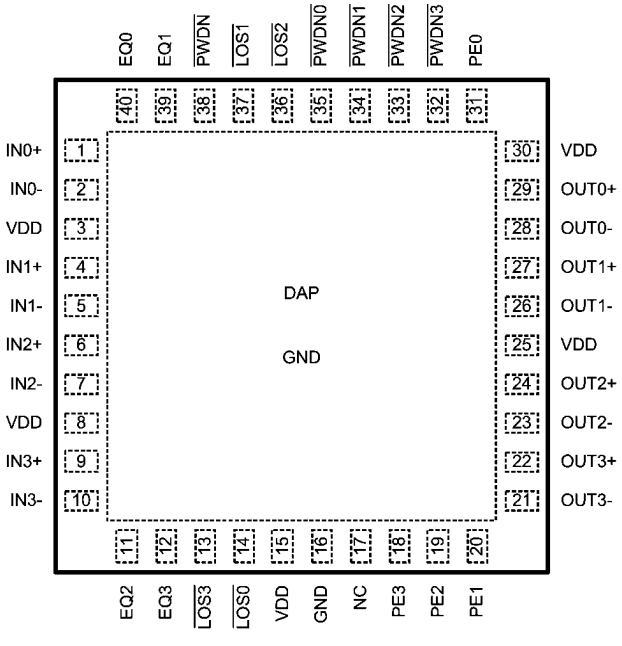
Connection Diagram



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DS25BR440 Pin Diagram

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0- , IN1+, IN1-, IN2+, IN2-, IN3+, IN3-	1, 2, 4, 5, 6, 7, 9, 10	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-	29, 28, 27, 26, 24, 23, 22, 21	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
EQ0, EQ1, EQ2, EQ3	40, 39, 11, 12	I, LVCMOS	Receive equalization level select pins.
PE0, PE1, PE2, PE3	31, 20, 19, 18	I, LVCMOS	Transmit pre-emphasis level select pins.
$\overline{\text{PWDN0}}$, $\overline{\text{PWDN1}}$, $\overline{\text{PWDN2}}$, $\overline{\text{PWDN3}}$	35, 34, 33, 32	I, LVCMOS	Channel output power down pins. When the $\overline{\text{PWDNn}}$ is set to L, the channel output OUTn is in the power down mode. The $\overline{\text{LOS}}$ circuitry on the corresponding input remains enabled.
$\overline{\text{LOS0}}$, $\overline{\text{LOS1}}$, $\overline{\text{LOS2}}$, $\overline{\text{LOS3}}$	14, 37, 36, 13	O, LVCMOS	Loss Of Signal output pins, $\overline{\text{LOSn}}$ report when an open input fault condition is detected at the input, INn. These are open drain outputs. External pull up resistors are required.
NC	17	NC	NO CONNECT pins. May be left floating.
$\overline{\text{PWDN}}$	38	I, LVCMOS	Device power down pin. When the $\overline{\text{PWDN}}$ is set to L, the device is in the power down mode. The $\overline{\text{LOS}}$ circuitry is disabled as well.
VDD	3, 8, 15,25, 30	Power	Power supply pins.
GND	16, DAP	Power	Ground pin and a pad (DAP - die attach pad).

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVCMOS Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage	−0.3V to +4V
LVDS Differential Input Voltage	0.0V to +1V
LVDS Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage	0.0V to +1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SQA Package	2.44W
Derate SQA Package	19.49 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+26.9°C/W
θ_{JC}	+3.8°C/W
ESD Susceptibility	
HBM (Note 1)	≥8 kV
MM (Note 2)	≥250V
CDM (Note 3)	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V V_{CC} = 3.6V		0	±10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND V_{CC} = 3.6V		0	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V		−0.9	−1.5	V
V_{OL}	Low Level Output Voltage	I_{OL}= 4 mA		0.26	0.4	V
LVDS INPUT DC SPECIFICATIONS						
V_{ID}	Input Differential Voltage	V_{CM} = +0.05V or V_{CC}-0.05V	0		1	V
V_{TH}	Differential Input High Threshold			0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = +3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current (Note 8)	OUT to GND		-35	-55	mA
		OUT to V_{CC}		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	PE = OFF, EQ = OFF $\overline{PWDN}$ = H		162	190	mA
I_{CCZ}	Power Down Supply Current	$\overline{PWDN}$ = L		55	63	mA

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 7: Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics (Notes 9, 10)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS							
t_{PLHD}	Differential Propagation Delay Low to High (Note 11)	R_L = 100Ω			390	600	ps
t_{PHLD}	Differential Propagation Delay High to Low (Note 11)				400	600	ps
t_{SKD1}	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (Notes 11, 12)				10	50	ps
t_{SKD2}	Channel to Channel Skew (Notes 11, 13)				18	65	ps
t_{SKD3}	Part to Part Skew (Notes 11, 14)				50	170	ps
t_{LHT}	Rise Time (Note 11)	R_L = 100Ω			80	160	ps
t_{HLT}	Fall Time (Note 11)				80	160	ps
t_{ON}	Any $\overline{PWDN}$ to Output Active Time				8	20	µs
t_{OFF}	Any $\overline{PWDN}$ to Output Inactive Time				5	12	ns
JITTER PERFORMANCE WITH EQ = Off, PE = Off (Note 11) **(*Figure 5*)**							
t_{RJ1}	Random Jitter (RMS Value) No Test Channels (Note 15)	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	2.5 Gbps		0.5	1	ps
t_{RJ2}			3.125 Gbps		0.5	1	ps
t_{DJ1}	Deterministic Jitter (Peak to Peak) No Test Channels (Note 16)	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		6	22	ps
t_{DJ2}			3.125 Gbps		10	29	ps
t_{TJ1}	Total Jitter (Peak to Peak) No Test Channels (Note 17)	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.04	0.09	UI_{P-P}
t_{TJ2}			3.125 Gbps		0.06	0.14	UI_{P-P}
JITTER PERFORMANCE WITH EQ = Off, PE = On (Note 11) **(*Figures 6*, *9*)**							
t_{RJ1B}	Random Jitter (RMS Value) Test Channel B (Note 15)	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	2.5 Gbps		0.5	1	ps
t_{RJ2B}			3.125 Gbps		0.5	1	ps
t_{DJ1B}	Deterministic Jitter (Peak to Peak) Test Channel B (Note 16)	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		7	15	ps
t_{DJ2B}			3.125 Gbps		4	23	ps
t_{TJ1B}	Total Jitter (Peak to Peak) Test Channel B (Note 17)	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.05	0.10	UI_{P-P}
t_{TJ2B}			3.125 Gbps		0.06	0.14	UI_{P-P}
JITTER PERFORMANCE WITH EQ = On, PE = Off (Note 11) **(*Figures 7*, *9*)**							
t_{RJ1D}	Random Jitter (RMS Value) Test Channel D (Note 15)	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	2.5 Gbps		0.5	1	ps
t_{RJ2D}			3.125 Gbps		0.5	1	ps
t_{DJ1D}	Deterministic Jitter (Peak to Peak) Test Channel D (Note 16)	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		14	30	ps
t_{DJ2D}			3.125 Gbps		15	30	ps
t_{TJ1D}	Total Jitter (Peak to Peak) Test Channel D (Note 17)	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.08	0.15	UI_{P-P}
t_{TJ2D}			3.125 Gbps		0.10	0.17	UI_{P-P}

Symbol	Parameter	Conditions		Min	Typ	Max	Units
JITTER PERFORMANCE WITH EQ = On, PE = On (Note 11) (***Figures 8, 9***)							
t_{RJ1BD}	Random Jitter (RMS Value)	V_{ID} = 350 mV	2.5 Gbps		0.5	1	ps
t_{RJ2BD}	Input Test Channel D Output Test Channel B (Note 15)	V_{CM} = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps
t_{DJ1BD}	Deterministic Jitter (Peak to Peak)	V_{ID} = 350 mV	2.5 Gbps		11	23	ps
t_{DJ2BD}	Input Test Channel D Output Test Channel B (Note 16)	V_{CM} = 1.2V K28.5 (NRZ)	3.125 Gbps		5	24	ps
t_{TJ1BD}	Total Jitter (Peak to Peak)	V_{ID} = 350 mV	2.5 Gbps		0.08	0.14	UI_{P-P}
t_{TJ2BD}	Input Test Channel D Output Test Channel B (Note 17)	V_{CM} = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.10	0.20	UI_{P-P}

Note 9: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 10: Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 13: t_{SKD2}, Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).

Note 14: t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 15: Measured on a clock edge with a histogram and an acummulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

Note 16: Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

Note 17: Measured on an eye diagram with a histogram and an acummulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

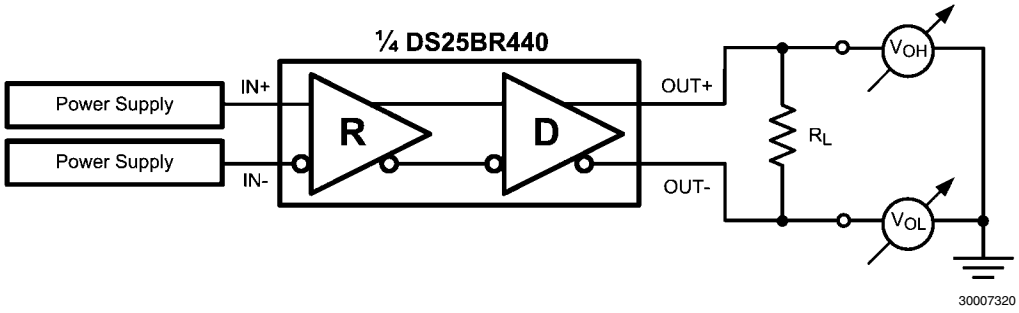


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

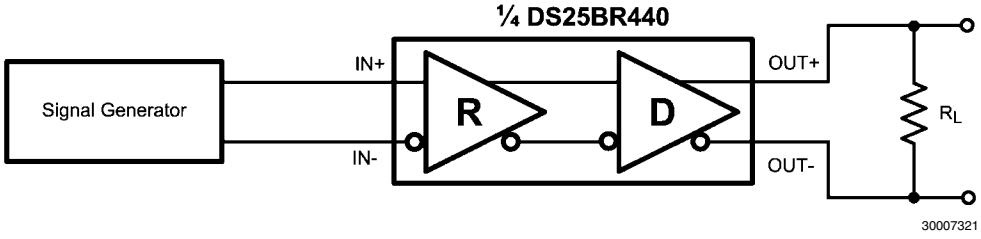


FIGURE 2. Differential Driver AC Test Circuit

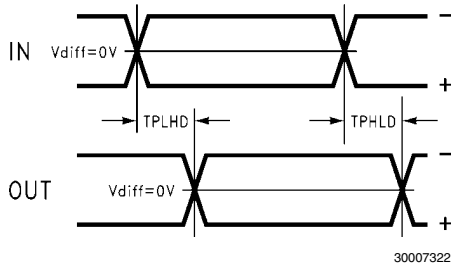


FIGURE 3. Propagation Delay Timing Diagram

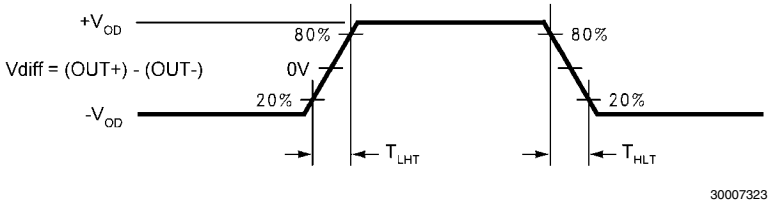


FIGURE 4. LVDS Output Transition Times

Pre-Emphasis and Equalization Test Circuits

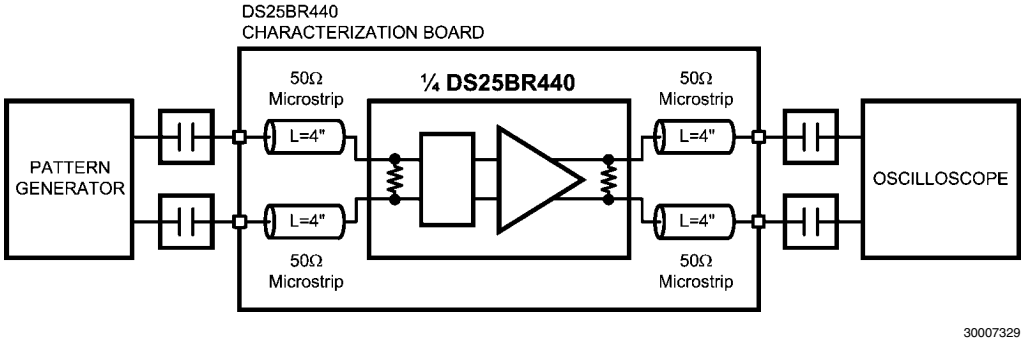


FIGURE 5. Jitter Performance Test Circuit

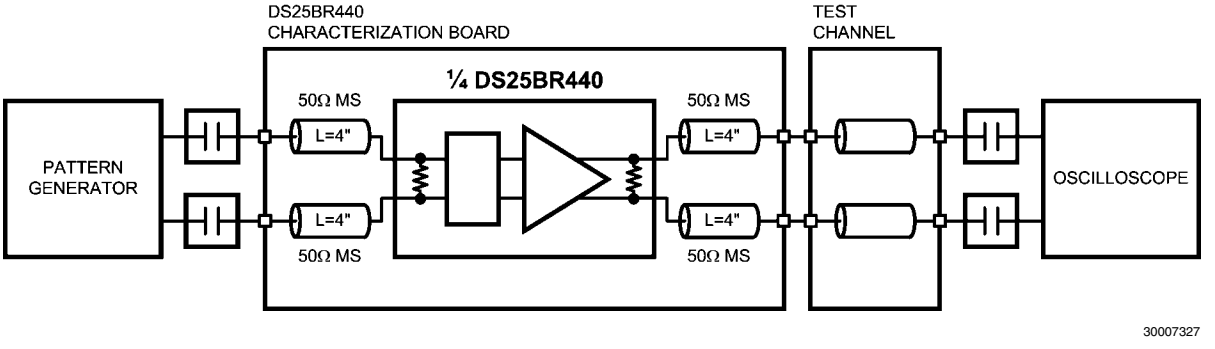


FIGURE 6. Pre-emphasis Performance Test Circuit

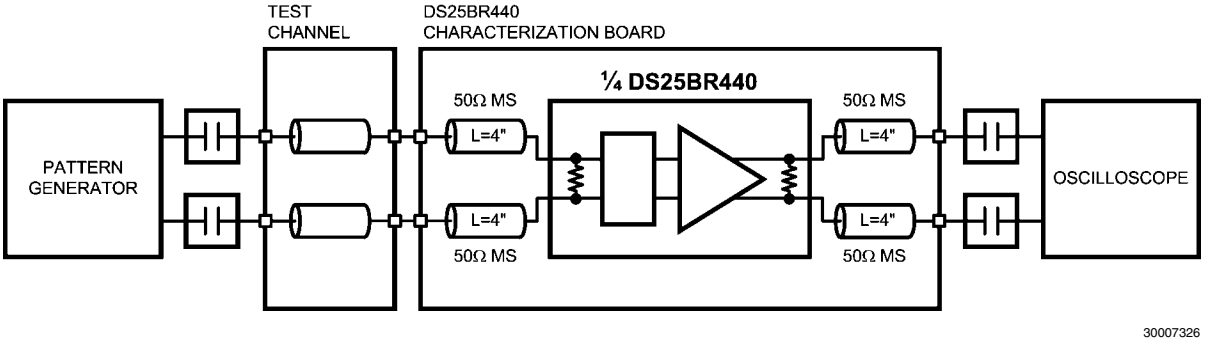


FIGURE 7. Equalization Performance Test Circuit

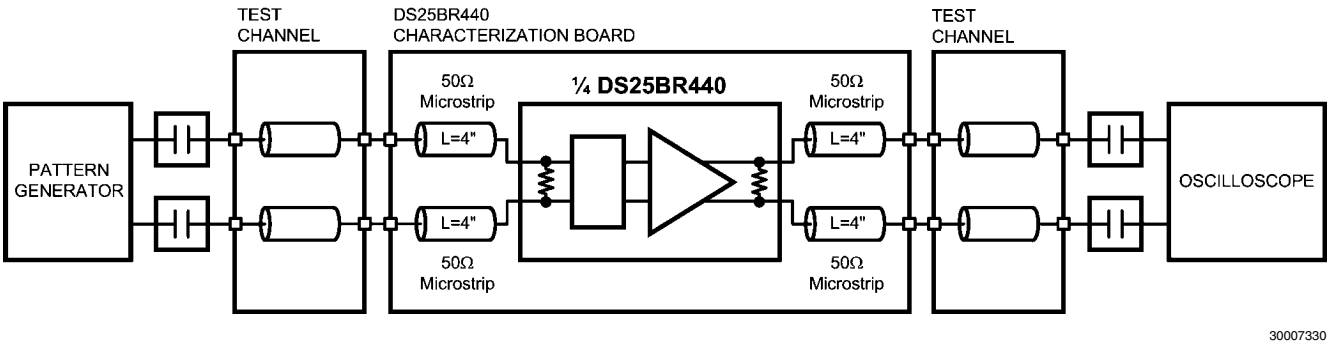


FIGURE 8. Pre-emphasis and Equalization Performance Test Circuit

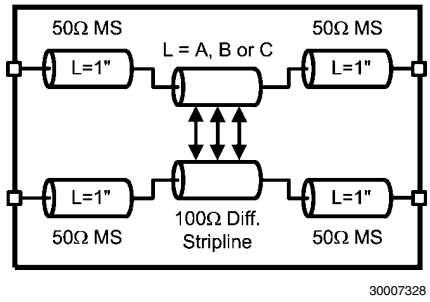


FIGURE 9. Test Channel Block Diagram

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Functional Description

The DS25BR440 is a 3.125 Gbps Quad LVDS buffer optimized for high-speed signal routing and repeating over lossy FR-4 printed circuit board backplanes and balanced cables.

The DS25BR440 has a pre-emphasis control pin for each output for switching the transmit pre-emphasis to ON and OFF setting and an equalization control pin for each input for switching the receive equalization to ON and OFF setting. The following are the transmit pre-emphasis and receive equalization truth tables.

Transmit Pre-emphasis Truth Table

OUTPUT OUTn, n = {0, 1, 2, 3}	
CONTROL Pin (PEn) State	**Pre-emphasis Level**
0	OFF
1	ON

Transmit Pre-emphasis Level Selection for an Output OUTn

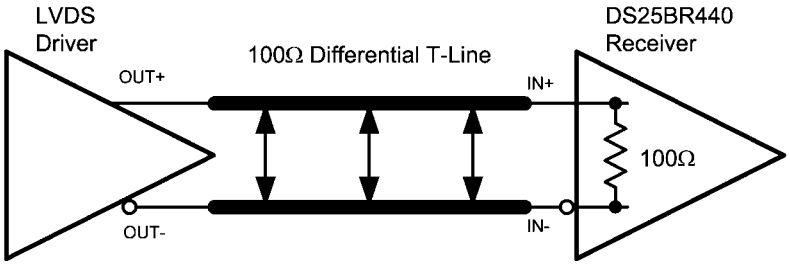
Receive Equalization Truth Table

INPUT INn, n = {0, 1, 2, 3}	
CONTROL Pin (EQn) State	**Equalization Level**
0	OFF
1	ON

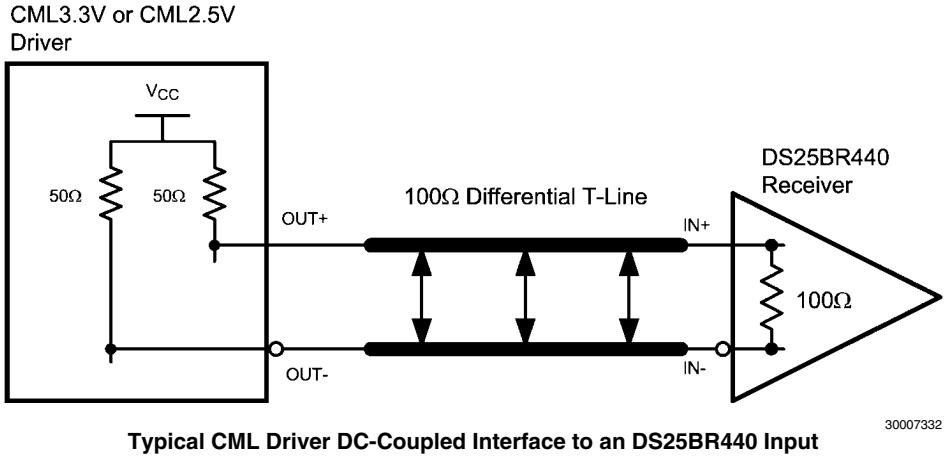
Receive Equalization Level Selection for an Input INn

Input Interfacing

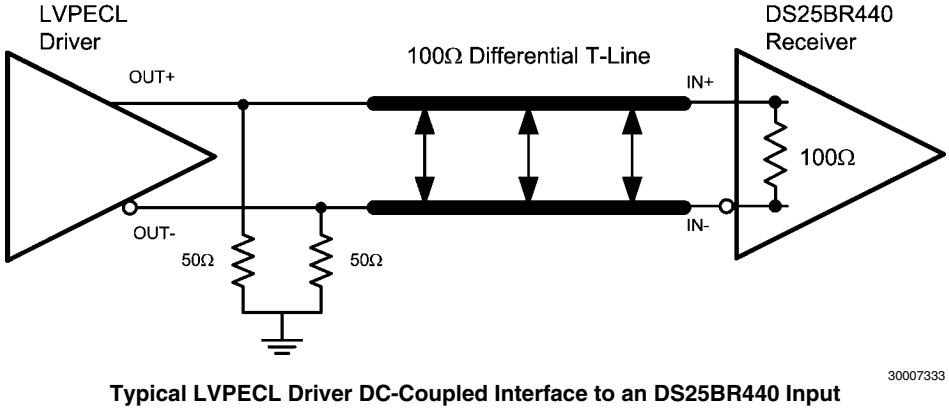
The DS25BR440 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR440 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR440 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to an DS25BR440 Input



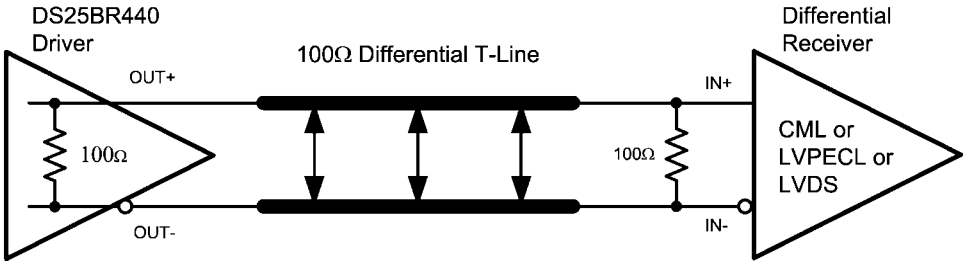
Typical CML Driver DC-Coupled Interface to an DS25BR440 Input



Typical LVPECL Driver DC-Coupled Interface to an DS25BR440 Input

Output Interfacing

The DS25BR440 outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



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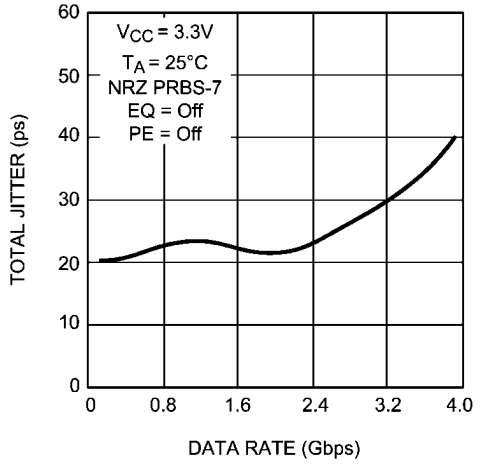
Typical DS25BR440 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance



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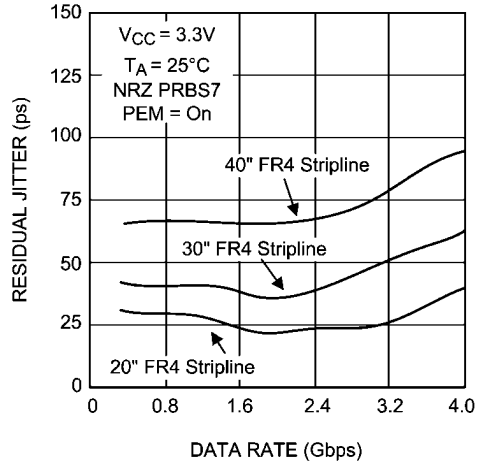
Total Jitter as a Function of Data Rate



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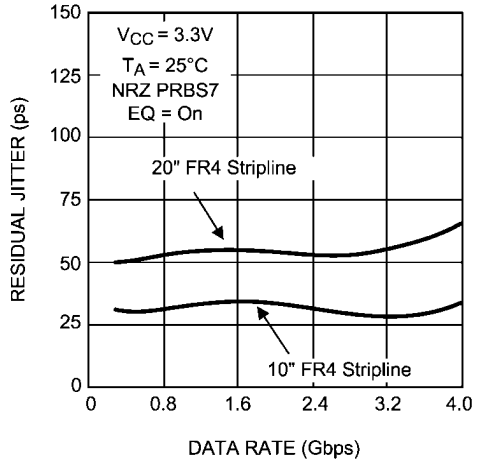
Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level



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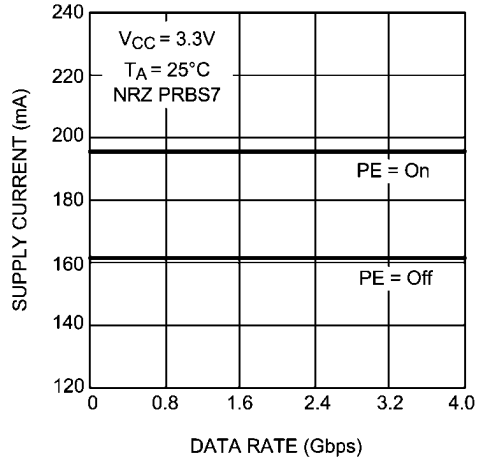
Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level



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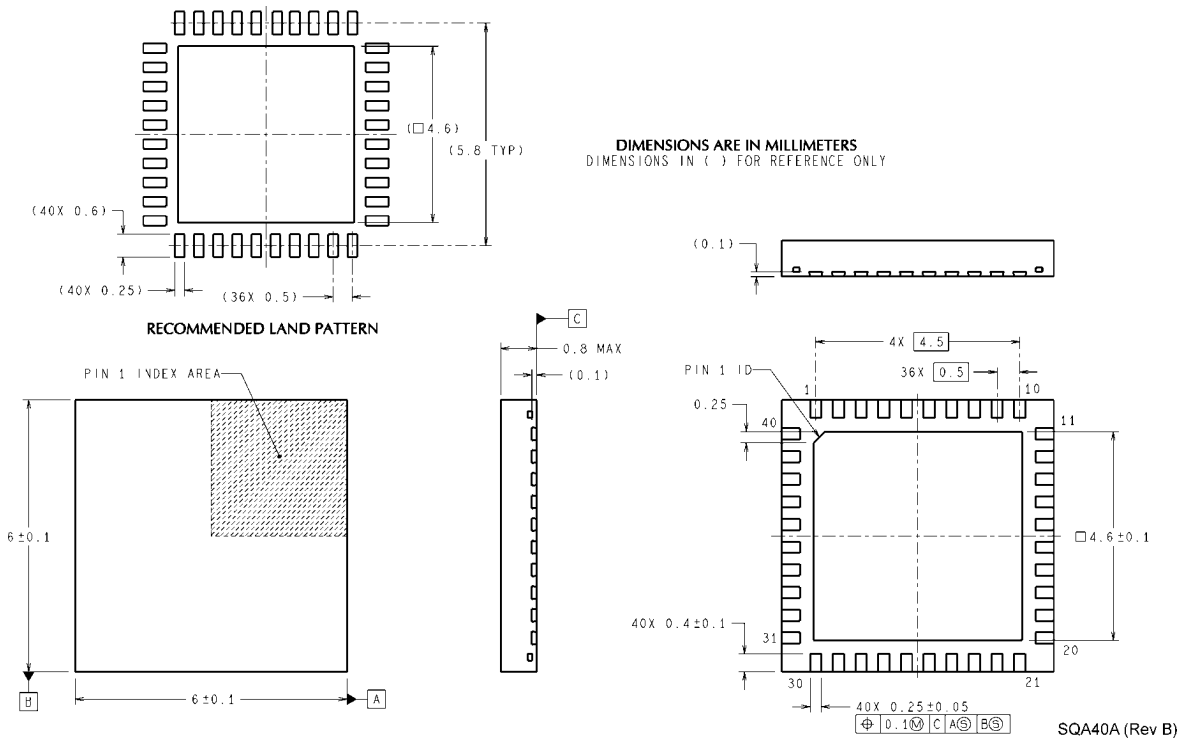
Supply Current as a Function of Data Rate and PE Level

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS25BR440TSQ
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(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

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